

FIG. 1



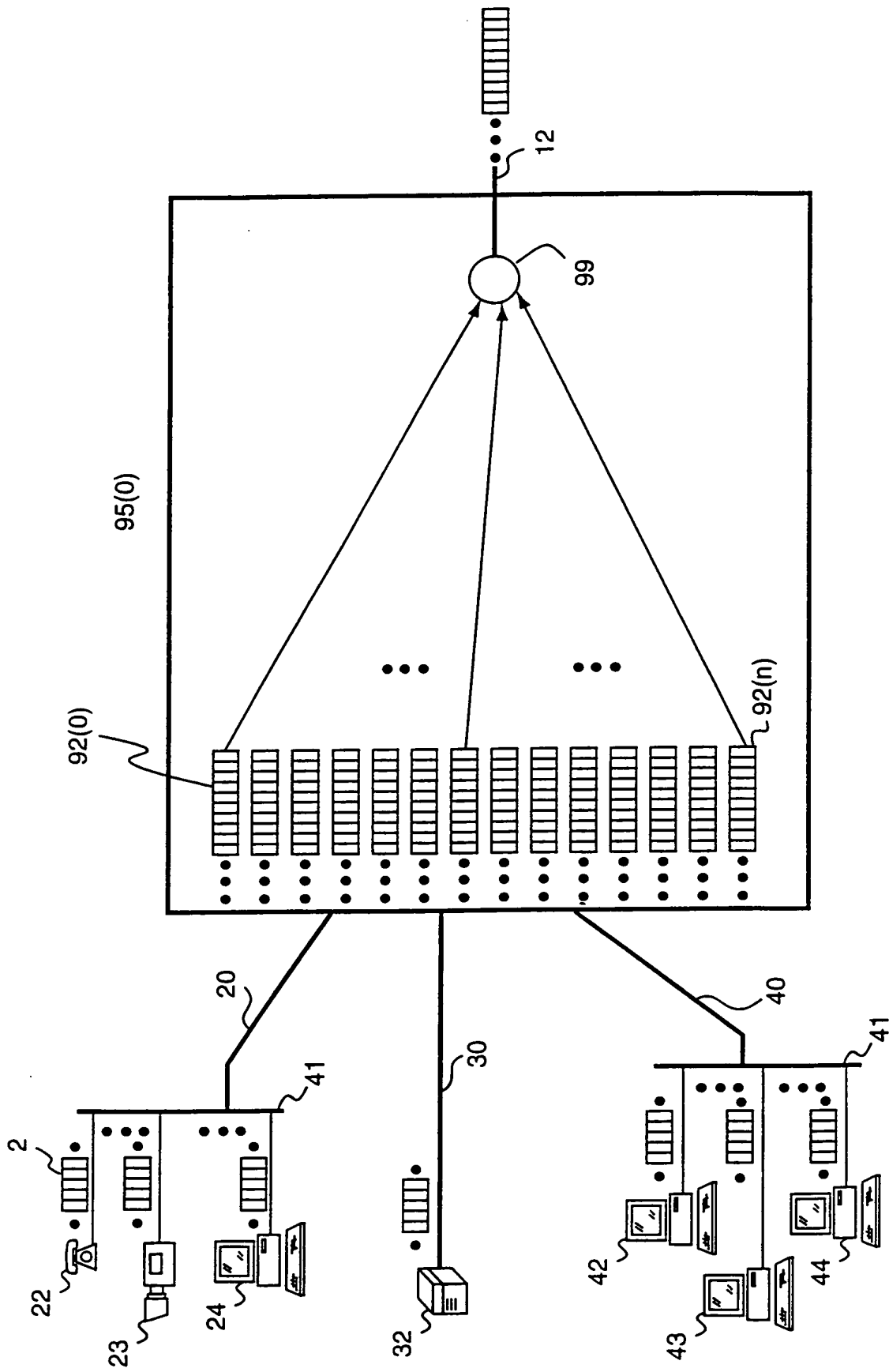


FIG. 3a

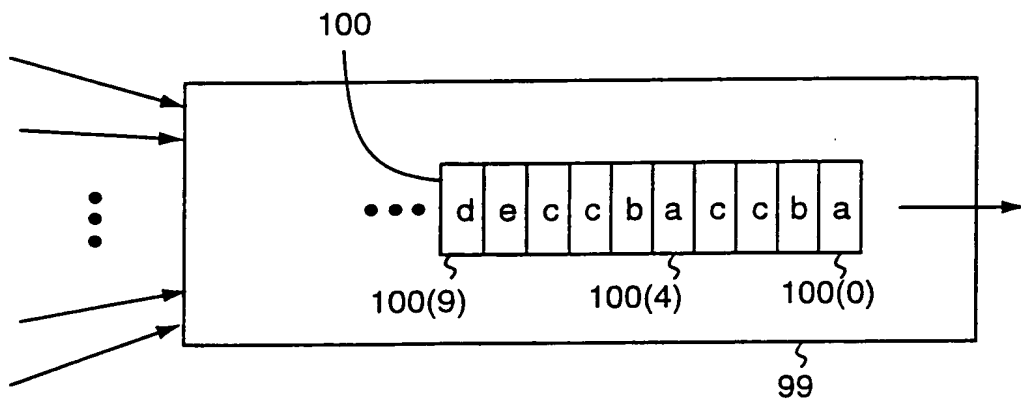


Fig. 3b

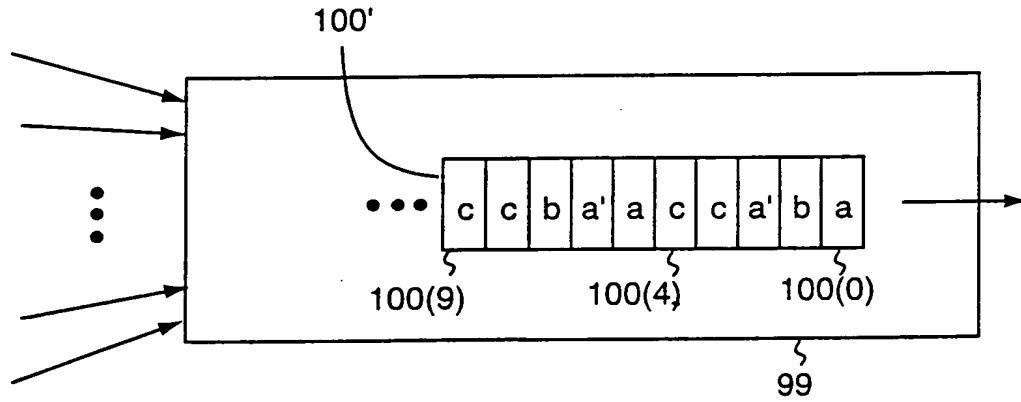


Fig. 3c

FIG. 4 is a block diagram of a parallel processing architecture 105. The architecture 105 includes a plurality of processing units 192(0) through 192(k) connected to a central processing unit 210. Each processing unit 192(i) includes a set of input registers 192(i,0) through 192(i,4) and a set of output registers 200(i,0) through 200(i,4). The processing units 192(i) are connected to the central processing unit 210 via a bus 212. The central processing unit 210 is connected to a memory unit 220.

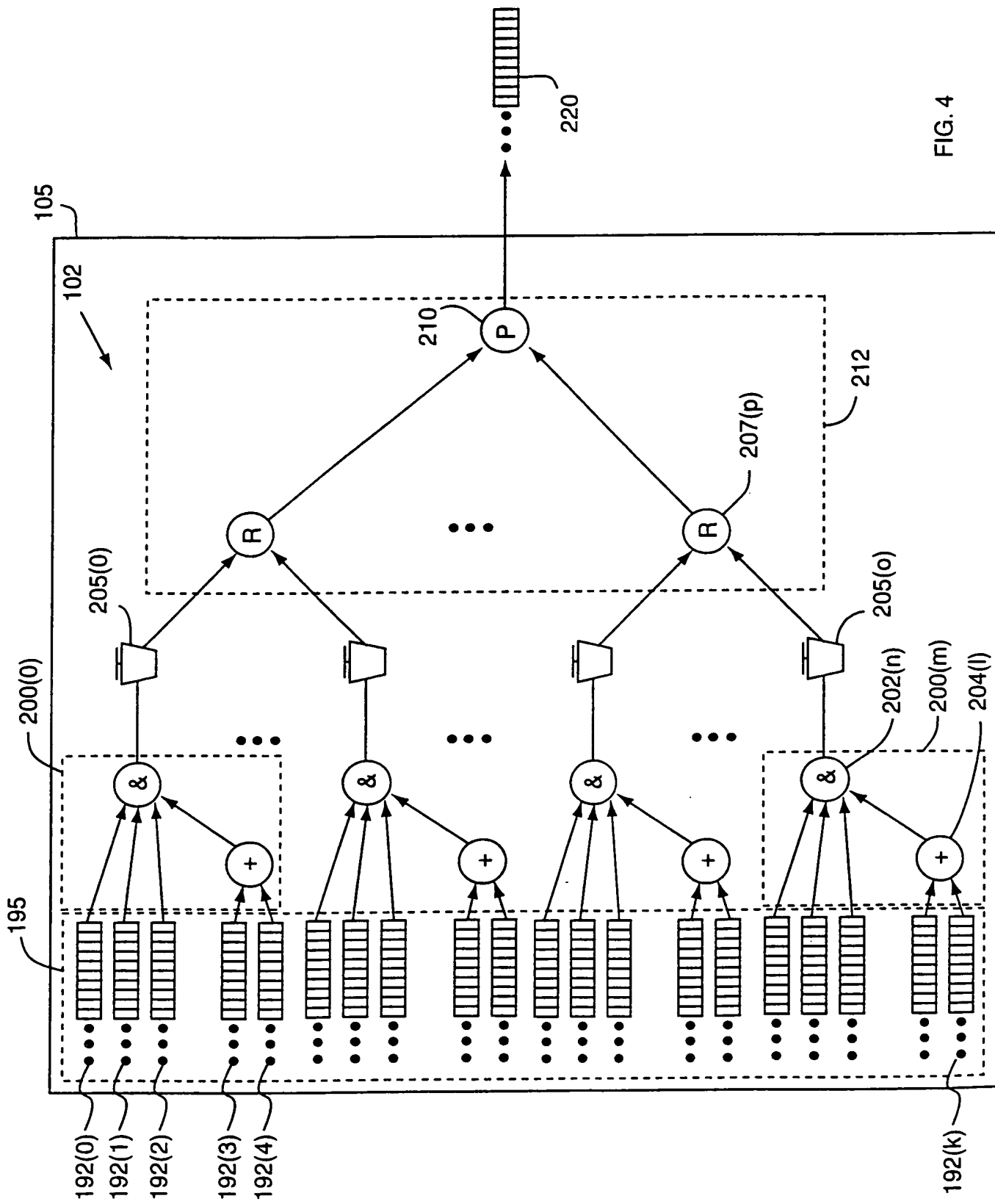
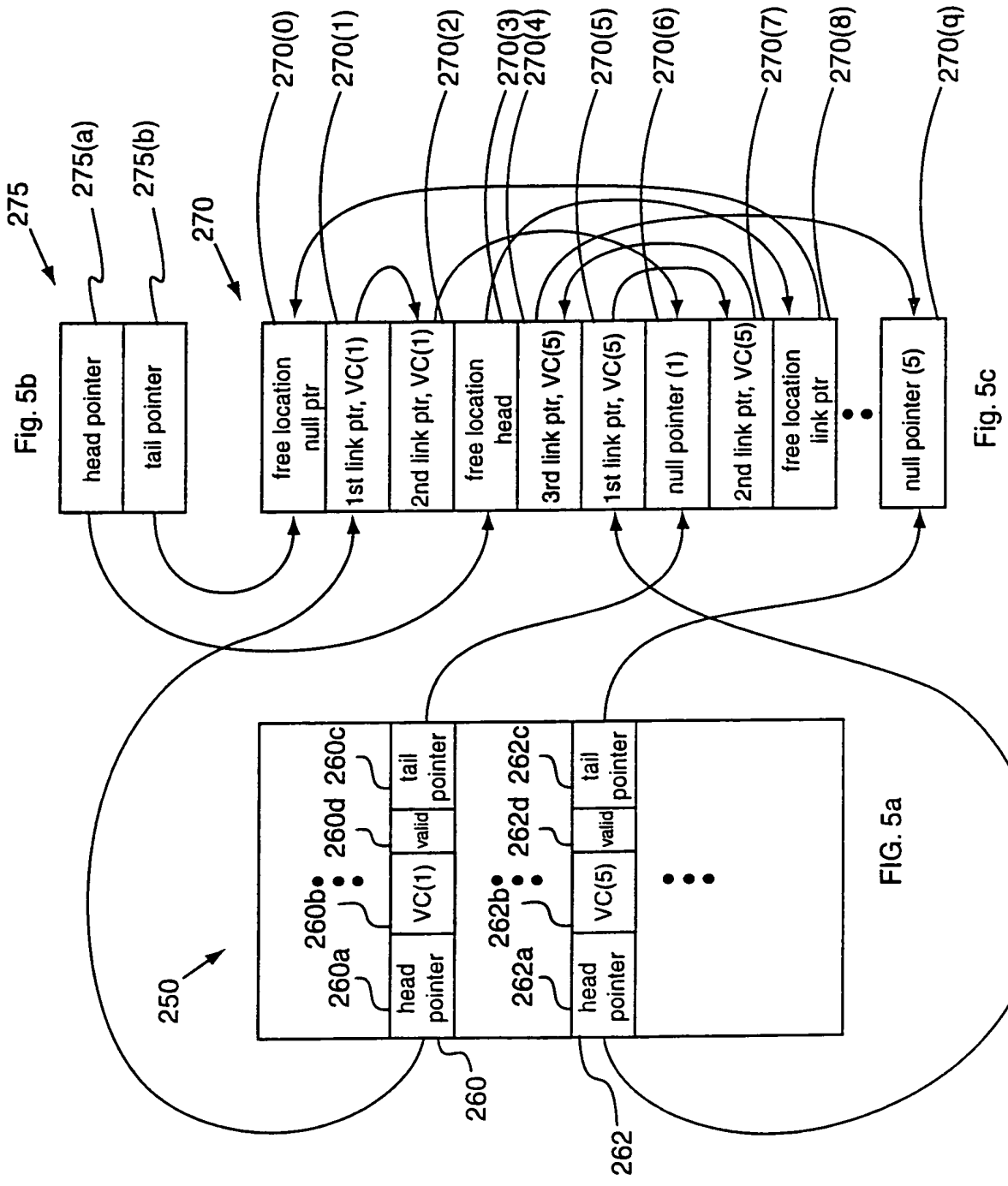


FIG. 4



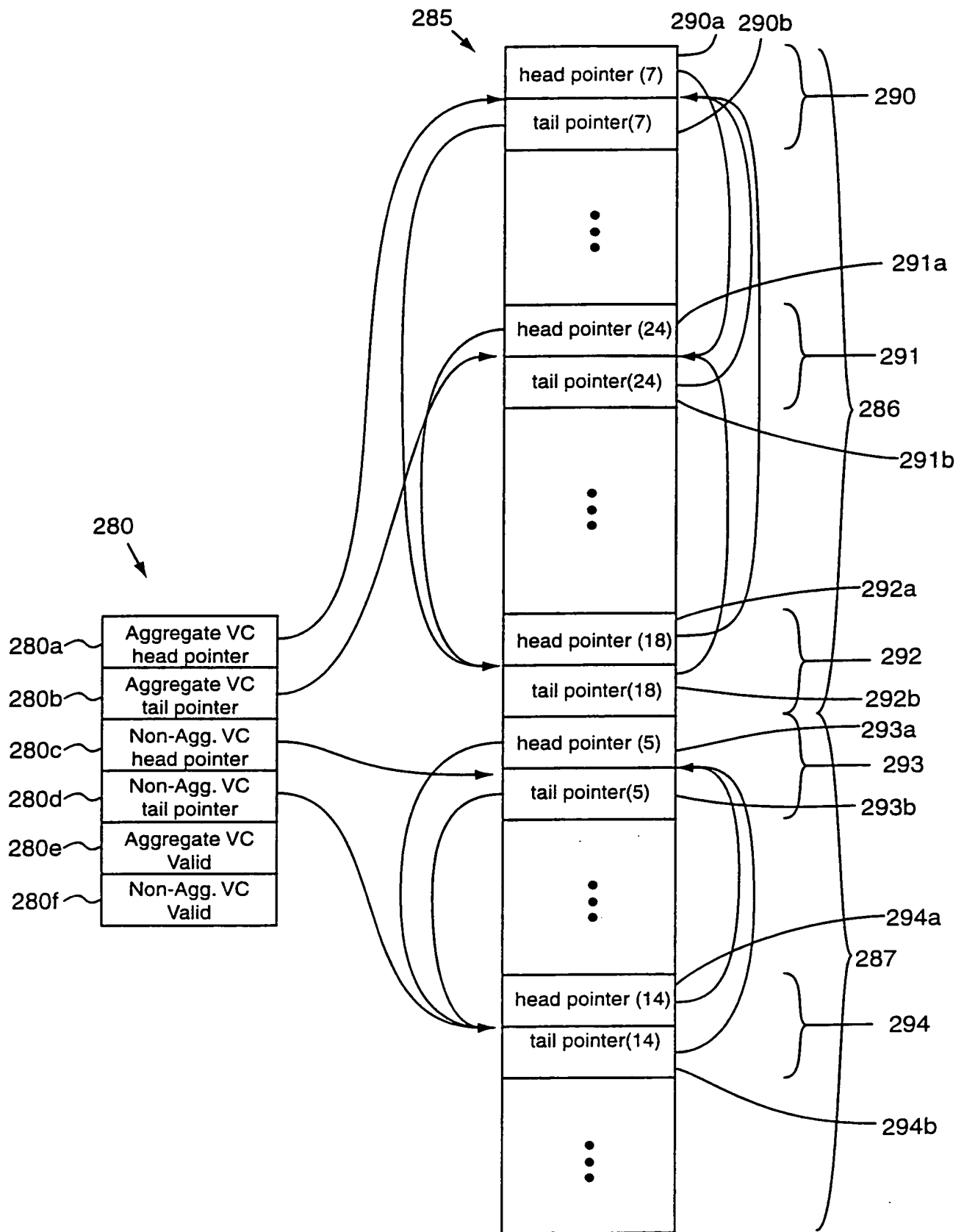


FIG. 6

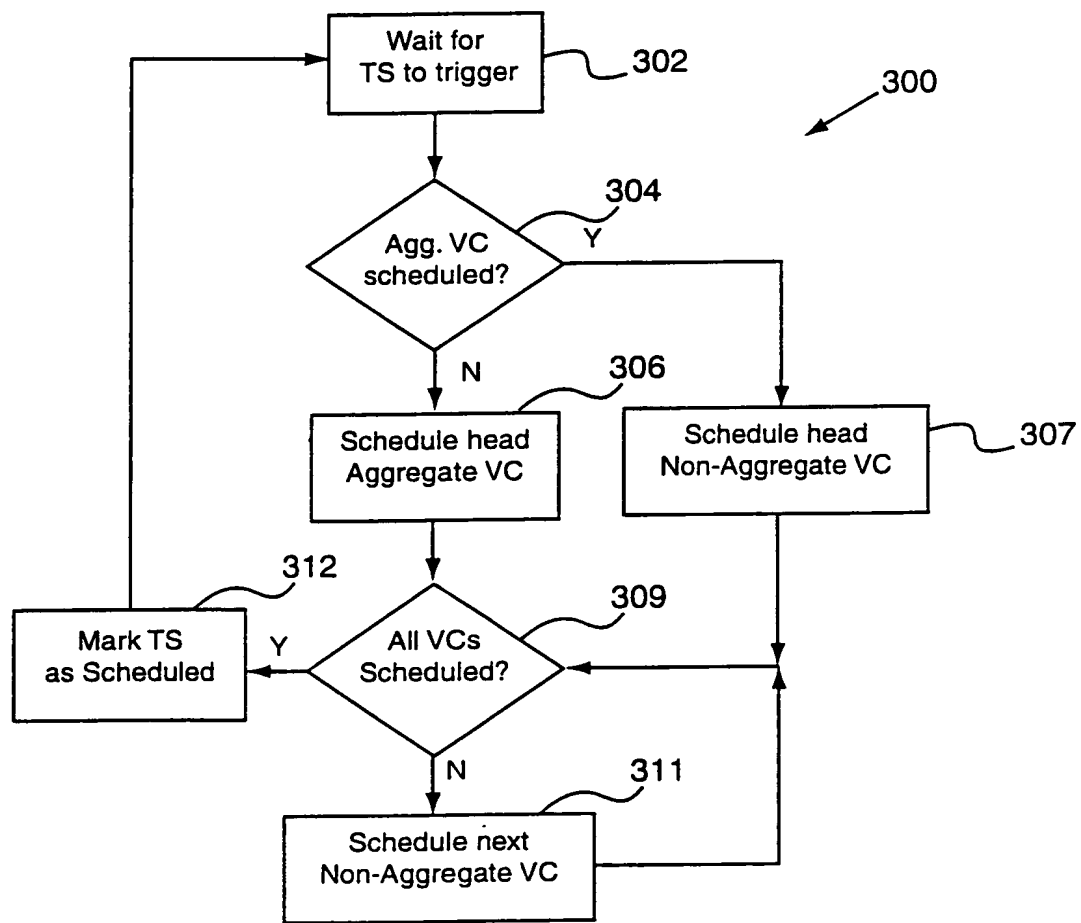


FIG. 7



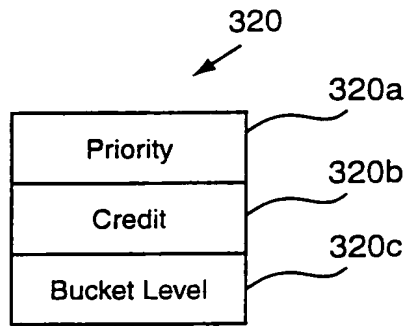


FIG. 8a

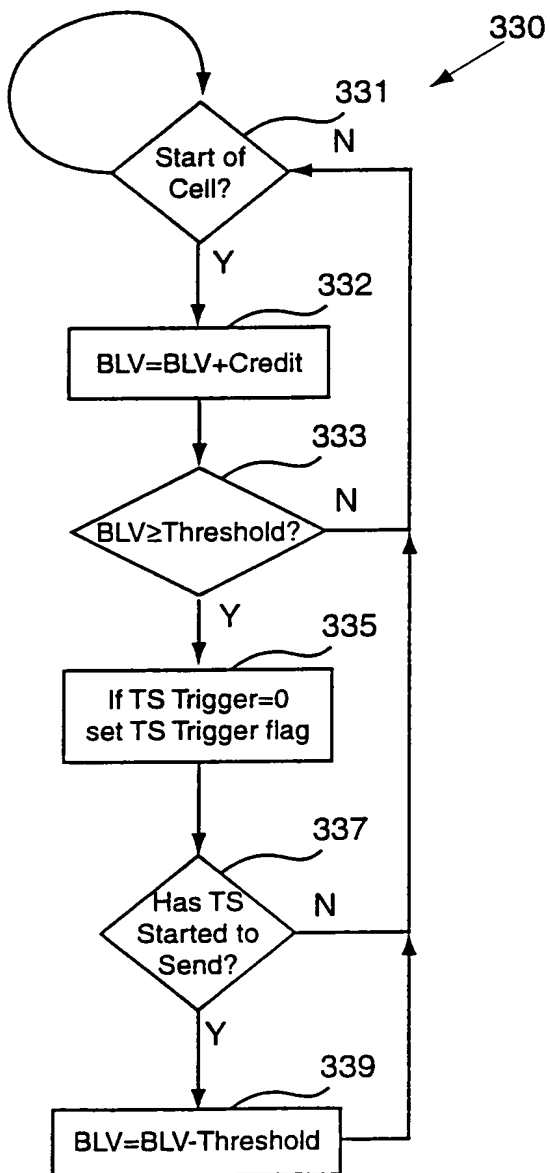


FIG. 8b

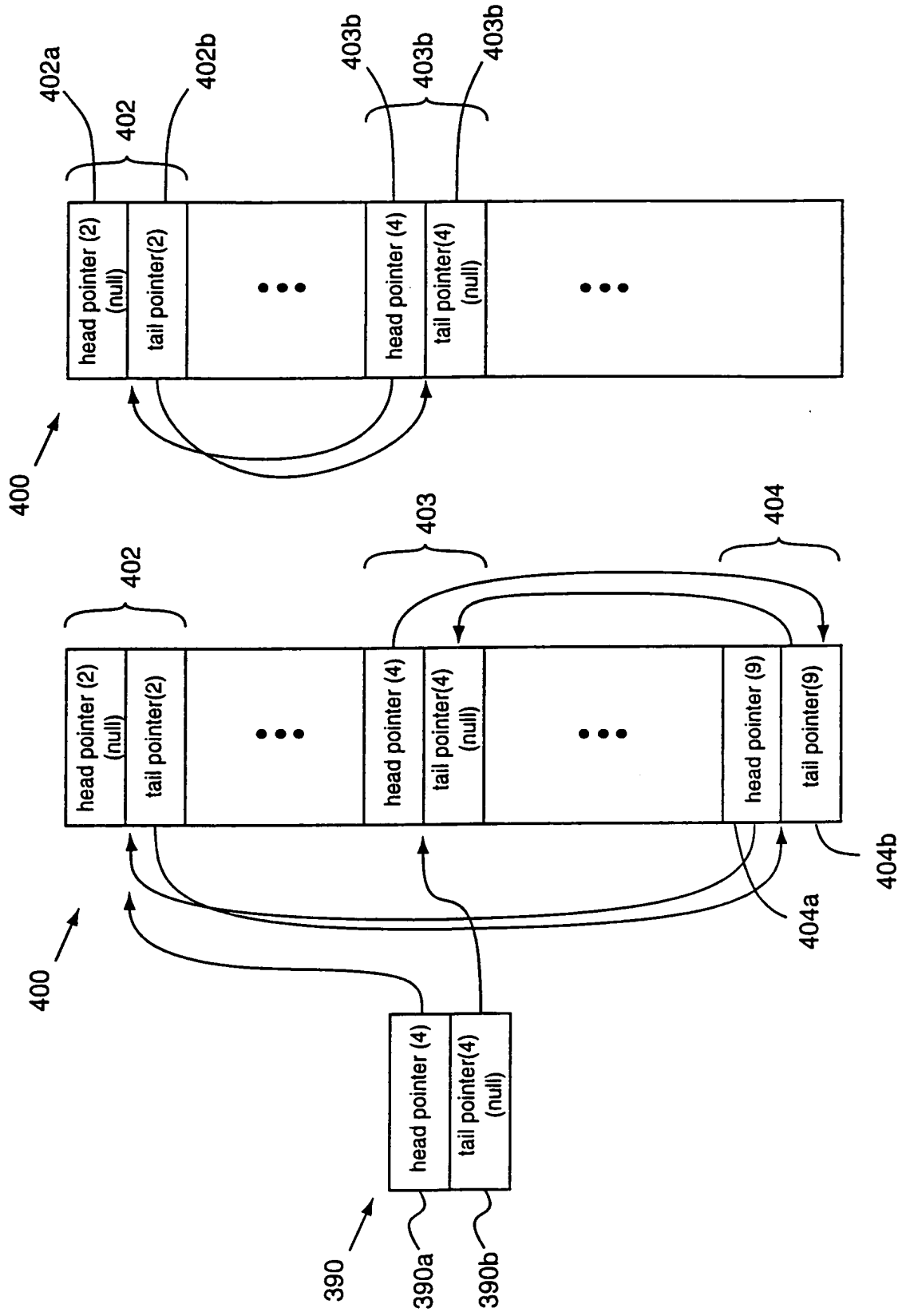


FIG. 9a

FIG. 9b

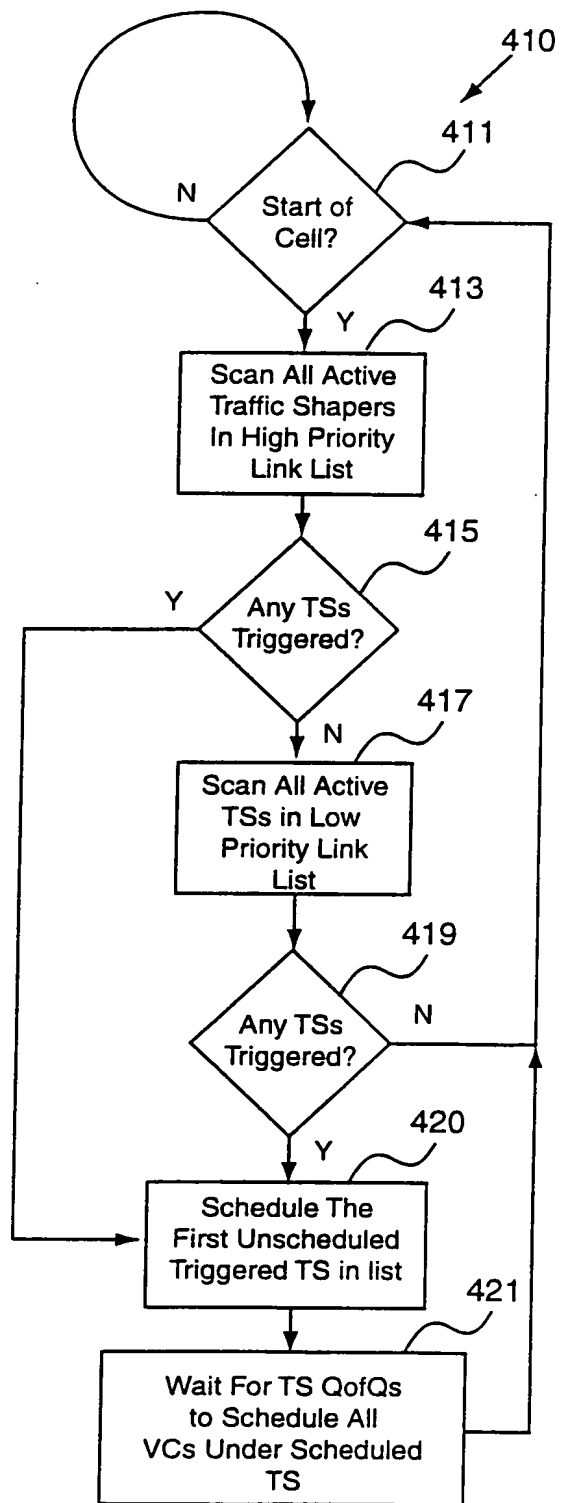


FIG. 10